WHAT IS CLAIMED IS:

sub a5

1. A signal router comprising:

a switching matrix, wherein said switching matrix has a first number of inputs and a second number of outputs;

an error detector, coupled to said one of said second number of outputs and configured to generate error information by virtue of being configured to detect errors in said information stream; and

a controller, coupled to said switching matrix and said error detector, wherein said controller is configured to

select a one of said first number of inputs from said first number of inputs,

receive error information from said error detector, and

configure said switching matrix to couple a one of said first number of inputs to a one of said second number of outputs, and

said switching matrix is configured to receive an information stream at said one of said first number of inputs.

2. The signal router of claim 1, further comprising:

a plurality of switching matrices, wherein

said switching matrix is one of said plurality of switching matrices,

said switching matrix is configured to identify said switching matrix by virtue of said error information generated by said error detector.

3. The signal router of claim 1, further comprising:

a plurality of error detectors, wherein

each one of said plurality of switching matrices is coupled to a corresponding one of said plurality of error detectors,

said switching matrix is configured to identify at least one of said plurality of switching matrices by virtue of said error information generated by a corresponding one of said plurality of error detectors, and

said at least one of said plurality of switching matrices experiences a failure detected by said corresponding one of said plurality of error detectors.

4. The signal router of claim 1, wherein said controller is further configured to reconfigure said switching matrix in response to said error information.

5. The signal router of claim 1, wherein said controller further configures said switching matrix to couple said one of said first number of inputs to another of said second number of outputs in addition to said one of said second number of outputs.

6. The signal router of claim 1, further comprising:

a plurality of receivers, each one of said plurality of receivers coupled to a corresponding one of said first number of inputs and including a receiver error detector configured to detect errors in a received information stream; and

a plurality of transmitters, each one of said plurality of transmitters coupled to a corresponding one of said second number of outputs and including a transmitter error detector configured to detect errors in an information stream to be transmitted, wherein said error detector further localizes a source of said errors by virtue of being configured to detect errors occurring after said receiver error detector of said each one of said plurality of receivers and before said transmitter error detector of said each one of said plurality of transmitters.

7. The signal router of claim 6, wherein said each one of said plurality of receivers is an optical receiver and said each one of said plurality of transmitters is an optical transmitter.

8. The signal router of claim 1, further comprising:

a clock/data recovery unit coupled between said one of said second number of outputs and said error detector; and

a demultiplexer coupled between said clock/data recovery unit and said error detector.

9. The signal router of claim 8, wherein said clock/data recovery unit comprises a phase-locked loop.

10. The signal router of claim 1, wherein said information stream comprises a plurality of frames and said error detector comprises:

an error checker, coupled to said switching matrix and said controller, wherein said error checker is configured to generate error check information, and

said error check information is included in said error information; and

a framing circuit, coupled to said switching matrix, said controller, and said error checker, and configured to

detect a start-of-frame condition for each one of said plurality of frames,

indicate said start-of-frame condition to said error checker,

detect an end-of-frame condition for each one of said plurality of frames,

indicate said end-of-frame condition to said error checker, and

detect framing error, said framing error included in said error information.

11. The signal router of claim 10, wherein said framing error is an error in a set of errors that includes a loss-of-frame error, an out-of-frame error, and a loss-of-signal error.

12. The signal router of claim 10, said error detector further comprising:
an integrator, coupled between said error checker and said controller, and
coupled between said framing circuit and said controller, wherein
said integrator is configured to determine an error rate,
said error rate is determined by counting said occurrence of said error during a period of time. and
said error information comprises said error rate.

13. The signal router of claim 10, wherein:
said error checker and said framing circuit are coupled to an error counter,
said error counter is configured to maintain an error count by virtue of being configured to count an occurrence of an error detected by at least one of said error checker and said framing circuit,
said controller is configured to reset said error counter, periodically read an error count from said error counter, and calculate an error rate based on said error count, said error information comprising said error count.

14. The signal router of claim 13, wherein:
said error detector further comprises an error limit register and a comparator,
said comparator is coupled to said error counter and said error limit register,
said controller is further configured to load an error limit into said error limit register, and periodically read said error count from and reset said error counter in response to a signal generated by said error detector,
said signal is generated by said comparator when said error count is equal to said error limit.

15. The signal router of claim 10, wherein:
said error checker and said framing circuit are coupled to an error counter,
said error counter is configured to
maintain an error count by virtue of being configured to count an occurrence of an error detected by at least one of said error checker and said framing circuit, and
reset said error count upon said error count being read,
said controller is configured to periodically read an error count from said error counter, and calculate an error rate based on said error count, said error information comprising said error count.

16. The signal router of claim 15, wherein:
said error detector further comprises an error limit register and a comparator,
said comparator is coupled to said error counter and said error limit register,
said controller is further configured to load an error limit into said error limit register, and periodically read said error count from said error counter in response to a signal generated by said error detector,
said signal is generated by said comparator when said error count is equal to said error limit.

17. The signal router of claim 10, wherein said information stream is a SONET stream and each one of said plurality of frames is in a SONET frame format.

18. The signal router of claim 10, wherein said error checker is a parity checker.

19. The signal router of claim 10, wherein
each one of said plurality of frames contains an error check entry, and

said error checker generates said error check information by analyzing a one of said plurality of frames and comparing a result of said analyzing to an error check entry of another of said plurality of frames.

20. An error detection method comprising:

sending a first command to a controller, said controller coupled to control a switching matrix and to an error detector, said command causing said controller to configure said switching matrix to couple a one of a plurality of inputs to a one of a plurality of outputs, said one of a plurality of inputs configured to receive an information stream and said one of a plurality of outputs coupled to said error detector;

generating error information by detecting errors, if any, in said information stream using said error detector; and

retrieving said error information from said error detector using said controller.

21. The method of claim 20, wherein said controller configures said switching matrix to couple a one of a plurality of inputs to another of a plurality of outputs in addition to said one of a plurality of outputs.

22. The method of claim 20, wherein said generating error information comprises:

clearing an error counter of said error detector;

starting an error timer; and

until said error timer reaches a terminal value, incrementing said error counter each time an error is detected by said error detector.

23. The method of claim 20, wherein said information stream comprises a plurality of frames and said detecting errors comprises:

generating a framing error if a framing circuit of said error detector detects an error in framing in said information stream, wherein said framing

circuit is coupled to and provides framing information to an error checker of said error detector;

if no said error in framing is detected, generating a check error for each erroneous frame of said plurality of frames that is processed by said error detector, said error checker detecting an error in said erroneous frame.

24. The method of claim 20, wherein each one of said plurality of frames is a SONET frame and said framing error is an error in a set of errors that includes a loss-of-frame error, an out-of-frame error, and a loss-of-signal error.

25. The method of claim 20, wherein said error checker is a parity checker and said check error is a parity error.

26. The method of claim 25, wherein

said plurality of frames are received by said error detector in a sequence,

said error checker generates parity information for a currently-processed frame of said plurality of frames, said currently-processed frame at a position in said sequence, and

said error checker compares said parity information to a parity entry in another of said plurality of frames.

27. The method of claim 26, wherein

each one of said plurality of frames is a SONET frame,

said parity entry is a B1 byte of said SONET frame, and

said another of said plurality of frames is at another position in said sequence, said another position in said sequence immediately subsequent to said position in said sequence.

28. A failure detection method comprising:

sending a command to a plurality of controllers, wherein

each one of said controllers is coupled to control a corresponding one of a plurality of switching matrices,

said each one of said controllers is coupled to control a corresponding one of a plurality of error detectors,

each one of said switching matrices is coupled to at least one other of said switching matrices,

said command causes said controller to configure said corresponding one of said switching matrices to couple a one of a plurality of inputs of said corresponding one of said switching matrices to a one of a plurality of outputs of said corresponding one of said switching matrices, and

said one of said inputs is configured to receive an information stream and said one of said outputs is configured to output said information stream by virtue of being coupled to said one of said inputs;

generating error information corresponding to said one of said plurality of information streams by detecting errors, if any, in said one of said plurality of information streams using said one of said plurality of information streams; and

identifying failed ones of said switching matrices by retrieving said error information corresponding to each one of said switching matrices.

29. The method of claim 28, wherein each one of a plurality of outputs of a first plurality of said switching matrices are coupled to a corresponding one of a plurality of inputs of a second plurality of said switching matrices.

30. The method of claim 28, wherein each one of said controllers configures said corresponding one of said switching matrices to couple said one of said inputs to another of said outputs in addition to said one of said outputs.

31. The method of claim 28, wherein said generating error information comprises:

clearing an error counter of said corresponding one of said error detectors;

starting an error timer in said one of said controllers; and

until said error timer in said one of said controllers reaches a terminal value, incrementing said error counter each time an error is detected by said corresponding one of said error detectors.

32. The method of claim 28, wherein said information stream comprises a plurality of frames and said detecting errors comprises:

generating a framing error if a framing circuit of said corresponding one of said error detectors detects an error in framing in said information stream, wherein said framing circuit is coupled to and provides framing information to an error checker of said corresponding one of said error detectors; and

if no said error in framing is detected, generating a check error for each erroneous frame of said plurality of frames that is processed by said error detector, said error checker detecting an error in said erroneous frame.

Add A1

Add B1